

JSKT200&JSKH200

Description

- 1) A package of series of two chips.
- 2) With high thermal conductivity DBC as the insulation.
- 3) Welding by vacuum welding technology, which provide high reliability.



Typical Application

DC motor control, temperature control and light control system.

Absolute Maximum Ratings (Packaged into modules, unless otherwise specified, T_{CASE}=25°C)

Barranatar	T. of O. of 1111		Values		
Parameter	Test Conditions	Symbol	20	22	Unit
Operating junction temperature range		Tj	-40~	-125	$^{\circ}$ C
Storage temperature range		T _{stg}	-40~125		$^{\circ}$ C
Repetitive peak off-state voltage	T _j =25℃	V _{DRM}	2000	2200	V
Repetitive peak reverse voltage	Tj=25℃	V _{RRM}	2000	2200	V
Non-repetitive peak off-state voltage	Tj=25℃	V _{DSM}	2100	2300	V
Non-repetitive peak reverse voltage	Tj=25℃	V _{RSM}	2100	2300	V
Average on-state current	Tc=85℃	I _{T(AV)} /I _{F(AV)}	200		Α
Peak on-state surge current	t _P =10ms V _R =0.6V _{RRM}	ITSM/IFSM	5400		Α
I ² t value for fusing	t _P =10ms V _R =0.6V _{RRM}	l ² t	145	000	A ² s
Critical rate of rise of on-state current	I _G =2×I _{GT}	dl/dt	150		A/µs
Insulation voltage	A.C 50Hz(1s/1min)	V _{ISO}	3600	/3000	V

Electrical Characteristics (Packaged into modules, unless otherwise specified, T_{CASE}=25°C)

Parameter	Test Conditions	Symbol	Values	Unit
Peak on-state voltage	I _T =600A t _P =380μs	V_{TM}	≤1.8	V
Threshold voltage	T _j =125℃	V _{TO}	≤0.9	V
Dynamic resistance	Tj=125℃	Rd	≤1.6	mΩ



	V _D =V _{DRM}				
Repetitive peak off-state current	Tc=25℃	I _{DRM1}	≤100	μA	
	Tc=125℃	I _{DRM2}	≤60	mA	
	V _R =V _{RRM}				
Repetitive peak reverse current	Tc=25℃	I _{RRM1}	≤100	μΑ	
	Tc=125℃	I _{RRM2}	≤60	mA	
Triggering gate current	V _D =12V R _L =30Ω	I _{GT}	20-120	mA	
Holding current	I _T =1A	lн	≤250	mA	
Latching current	Ig=1.2 Igт	IL	≤300	mA	
Triggering gate voltage	V _D =12V R _L =30Ω	V _{GT}	≤1.8	V	
Non triggering gate voltage	$V_D=V_{DRM} T_j=125^{\circ}C$	V _{GD}	≥0.25	V	
Critical rate of rise of voltage	V _D =2/3V _{DRM} T _j =125℃ Gate Open	dv/dt	≥1000	V/µs	
Thermal resistance	Junction to case	R _{th(j-c)}	0.12	°C/W	
	Case to heatsink	R _{th(c-s)}	0.08		

Mechanical Characteristics

Module height Terminal distance of (1) /(2) /(3) Mounting torque(M5) Terminal torque(M6)	30.3mm 23mm 5±15%Nm		
Mounting torque(M5) Terminal torque(M6)			
Terminal torque(M6)	5±15%Nm		
916,05			
316.02	5±15%Nm		
94.05 94.05 3.3.05 3.3.05 3.3.05	(6) (7) (2) (3) (1) (4) (5) K1 JSKT symbol (1) (2) (3) (4) (5) K1 JSKH symbol		



Instructions and Precautions

- 1) There is no severe vibration and shock in operating environment, and there should be no impurity and atmosphere which may corrode metal and damage the insulation in the air-dielectric.
- 2) The operating condition of the product can't out of range of the above parameters.
- 3) When the product is installed on the radiator, the radiator's surface should be confirmed flat, smooth, wipe clean with alcohol, and coated evenly with a layer of thermal grease which thickness is moderate on the contact surface between product and radiator. When the module is fastened on the surface of the radiator, the M5 or M6 screws and spring washers are used and fastened with 5NM torque. After the module is operated 1 hour, all screws must be refastened.
- 4) The connection with the main electrode of module can use copper, welding, socket and so on. The contact surface should be smooth and flat, which make good contact. While the connection with the control electrode of module is installed, attention should be paid to the corresponding connection of each pin. After the completion of the connection, do not plug and pull out the lead of the control electrode freely.

Ordering Information

JS KT 200 / 22

JieJie Semiconductor Co.,Ltd

KT: Thyristor module

KH: Thyristor and diode module

KT: Thyristor and diode module

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Performance Curves

FIG.1:Power dissipation vs. on-state current (per thyristor or diode)

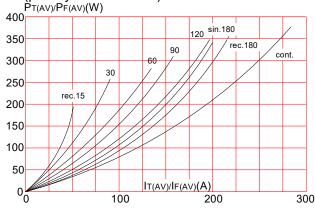


FIG.2: Maximum transient thermal impedance junction to case(per thyristor or diode)

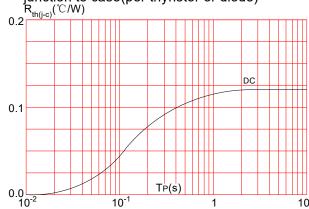




FIG.3:Forward characteristics (per thyristor or diode)

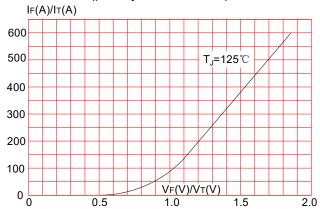
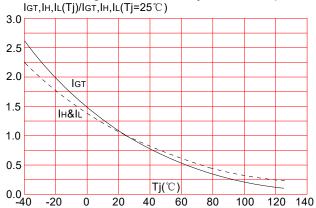


FIG.4: Relative variations of gate trigger current, holding current and latching current versus junction temperature



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